

11/13/03

SHEET 1 OF 1

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	ATTY. DOCKET NO. MICRON.271A	APPLICATION NO. Unknown 10/712,212
	APPLICANT Smith, et al.	
	FILING DATE Herewith	GROUP Unknown 2815

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)	

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
OK	Yanagisawa, et al.; TRENCH TRANSISTOR CELL WITH SELF-ALIGNED CONTACT (TSAC) FOR MEGABIT MOS DRAM; 1st LSI Division, NEC Corporation; 1120 Shimokuzawa, Sagamihara, Kanagawa 229, Japan; Pages 132-135.
OK	Landgraf, et al.; SCALABLE HIGH VOLTAGE TRENCHGATE TRANSISTOR FOR FLASH; University of Regensburg, Conference: ESSDERC 2000; 93040 Regensburg, Germany; Pages 380-383.
OK	Hieda, et al.; SUB-HALF-MICROMETER CONCAVE MOSFET WITH DOUBLE LDD STRUCTURE; IEEE Transactions on Election Devices, Vol. 39, No. 3, March, 1992, Pages 671-676.
	Sakao, et al. A STRAIGHT-LINE TRENCH ISOLATION AND TRENCH GATE TRANSISTOR (SLIT) CELL FOR GIGA-BIT DRAMS; ULSI Device Development Laboratories, NEC Corporation; 1120, Shimokuzawa, Sagamihara, Kanagawa 229, Japan; Pages 19 and 20. <i>No date</i>

MT/YR
*/1986
*/2000

H:\DOCS\IKJL\JL-2486.DOC/mng
111303

* No month cited.

EXAMINER <i>Dr. W. J. L.</i>	DATE CONSIDERED <i>2/28/05</i>
*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.	